REMARKS

This application has been carefully reviewed in light of the Official Action mailed on December 13, 2002. Applicant amends Claims 1, 11, and 32. Applicant respectfully requests reconsideration and favorable action in this case.

Information Disclosure Statement

As requested by the Examiner, copies of the IDS references previously submitted to the Examiner by Applicant on July 1, 2002 are included with this response, together with a clean copy of a form PTO-1449. Because these reference have already been properly and timely submitted to the Examiner at least once before, as described in Applicant's letter dated November 6, 2002, Applicant believes that no fee is due.

Section 103 Rejections

The Examiner rejects Claims 1-5 and 7-30 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,350,484 issued to Gardner, et al. ("*Gardner*") in view of U.S. Patent No. 5,736,002 issued to Allen, et al. ("*Allen*"). Applicant respectfully traverses these rejections for the reasons provided below.

Claim 18 is allowable because a combination of the references does not show "exposing the electronic device to a plasma and at least one other gas selected from the group of inert gases and nitrogen, the plasma converting an unmasked portion of the conductive layer into a compound and the at least one other gas enhancing the conversion into the compound . . . ." as recited by Claim 18; indeed, the Examiner makes no attempt to show that the cited references disclose the missing limitation.[1] The various gases listed in Tables 2 through 6 of *Gardner* are disclosed as means of **removing** an already formed compound. (See Column 8, lines 33-36). Similarly, *Allen* discloses only gases that are used to remove an already formed compound. Neither *Gardner* nor *Allen* discloses "exposing the electronic device to . . . at least one other gas selected form the group of inert gases and nitrogen . . . [for] enhancing the **conversion into** the compound . . . ." [emphasis added]. In some

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[1] The Office Action is completely devoid of any discussion regarding this limitation. Rather, the Examiner makes only a bare assertion on page 3 of the Office Action that the cited references disclose the limitations of Claim 18 ("Pertaining to claims 1, 11 and 18, Gardner discloses a semiconductor process substantially as claimed."). This clearly falls below the M.P.E.P standard that the Examiner is required to meet to properly reject a claim. For at least this reason, Claim 18 is allowable.

embodiments, this is advantageous because the speed of compound formation may be either increased to speed up the compound formation or decreased to better control the shape of a conductive layer. Because the combination of the cited references does not disclose the missing limitation, nor does the Examiner assert that it does, Claim 18 is allowable. Reconsideration and favorable action are requested.

Claim 1 is allowable over a combination of *Allen* and *Gardner* because the combination does not teach or suggest "exposing the semiconductor device to a plasma using a plasma deposition reactor, the plasma converting the unmasked portions of the conductive layer into a compound," as recited by Claim 1. *Allen* discloses forming compounds using a **plasma etcher**, not a **plasma deposition reactor**. For example, Column 9, lines 27-33 discloses a Lam Research 9600™ Transformer Coupled Plasma Metal Etcher, which is a plasma etcher, not a plasma deposition reactor of Claim 1. In fact, *Allen* is completely devoid of any mention of a plasma deposition reactor. As stated in the previous response dated July 1, 2002, *Gardner* also fails to show such a device.[2] Additionally, one skilled in the art would not be motivated to modify *Allen* to use a plasma deposition reactor instead of the plasma etcher because the two devices are designed to perform completely opposite functions; whereas a plasma etcher is used to ***remove*** a layer, a plasma deposition reactor is used to ***form*** a layer. Also, whereas a plasma deposition reactor operates in an energy range of approximately 30 volts or less, a plasma etcher operates in an energy range of approximately 50 to 100 volts. Thus, one skilled in the art would not be motivated to modify *Allen* to use a plasma deposition reactor because a plasma deposition reactor would not provide the higher level of energy provided by a plasma etcher. In some embodiments, exposing the semiconductor device to a plasma using a plasma deposition reactor reduces the power density to approximately 30 volts or less during the formation of the compound. Reducing

[2] As stated in the previous response dated July 1, 2002, *Gardner* involves either ion implantation or reactive ion etching (see Abstract and Claims). Ion implantation does not include exposing a device to a plasma. Reactive ion etching includes high energy plasma, and in *Gardner*, relies principally on ion bombardment to form the copper compound that will be removed. In contrast, exposing a semiconductor device to plasma by a plasma deposition reactor involves lower energy plasma, which relies principally on a chemical reaction to form the copper compound that will be removed. Because *Gardner* involves only high energy plasma it clearly does not show the use of a plasma deposition reactor, nor would it be obvious to modify *Gardner* to use a plasma deposition reactor. Because *Gardner* focuses on ion bombardment as the mechanism to create the compound, one would not have been motivated to use a plasma deposition reactor with *Gardner*, as such a plasma deposition reactor would not create the high energy plasma required.

the power density is advantageous in some embodiments because a lower power density reduces the probability of damage to the exposed semiconductor device. Because the combination of the cited references does not disclose the missing limitation of Claim 1, Claim 1 is allowable. Reconsideration and favorable action are requested.

Claim 11 is allowable over the cited references for reasons analogous to those provided in conjunction with Claims 18 and 1. Specifically, the cited references do not disclose "exposing the electronic device to a plasma using a plasma deposition reactor and at least one other gas selected from the group of inert gases and nitrogen, the plasma converting the unmasked portions of the conductive layer into a compound and the at least one other gas enhancing the conversion into the compound . . . ." as recited by Claim 11. Reconsideration and favorable actions are requested.

As depending from allowable independent Claims 1, 11, and 18, the respective dependent Claims 2-10, 12-17, and 19-30 are also allowable. Reconsideration and favorable action are requested.

<u>Section 102 Rejections</u>

The Examiner rejects Claims 31 and 32 under 35 U.S.C. § 102(b) as being anticipated by *Allen*. Applicant respectfully traverses these rejections for reasons provided below.

Claim 31 is allowable because *Allen* does not show "exposing, by a plasma deposition reactor, the device to a plasma, the plasma converting the unmasked portion of the conductive layer into a compound . . .." as recited by Claim 31. The Examiner identifies a plasma metal etcher at Column 9, line 28 of *Allen* as showing a plasma deposition reactor of Claim 31. This is incorrect because a plasma etcher and a plasma deposition reactor are two different devices designed to perform completely opposite functions; whereas a plasma etcher is used to ***remove*** a layer, a plasma deposition reactor is used to ***form*** a layer. Also, whereas a plasma deposition reactor operates in an energy range of approximately 30 volts or less, a plasma etcher operates in an energy range of approximately 50 to 100 volts, as described above in conjunction with Claim 1. Because *Allen* does not show the missing limitation, Claim 31 is allowable.

Claim 32 is allowable over *Allen* because *Allen* does not teach or suggest "exposing the device to a plasma having an energy level of approximately 30 volts or below, the plasma

converting the unmasked portion of the conductive layer into a compound. . . ." as recited by Claim 32. Support for the amendment of Claim 32 is provided at page 8, lines 21-29. It is respectfully submitted that one skilled in the art would understand that plasma deposition is one example of utilizing a plasma having an energy level of approximately 30 volts or below. As described above, the use of a plasma having an energy level of approximately 30 volts or below is not suggested or disclosed in *Allen* because *Allen* discloses compound formation using a plasma etcher, which requires an energy use of approximately 50 to 100 volts. Because *Allen* does not teach the missing limitation of Claim 32, Claim 32 is allowable. Reconsideration and favorable action are requested.

CONCLUSION

Applicant has now made an earnest attempt to place this case in condition for immediate allowance. For the foregoing reasons and for other apparent reasons, Applicant respectfully requests full allowance of all pending claims.

If Examiner believes that prosecution of this Application would be advanced by discussing the Application with Applicant's representative, a telephone call to the undersigned is strongly encouraged.

No additional fee is believed to be due. However, the Commissioner is hereby authorized to charge any fee or credit any overpayment to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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MARKED UP VERSION OF SPECIFICATION AND CLAIM AMENDMENTS

For the convenience of the Examiner, all claims have been presented whether or not an amendment has been made. The claims have been amended as follows:

1. **(Amended)** A method for forming a conductive pattern for a semiconductor device, comprising:

patterning a mask layer outwardly from a conductive layer of the semiconductor device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the semiconductor device to a plasma **<u>using a plasma deposition reactor</u>**, the plasma converting the unmasked portions of the conductive layer into a compound;

exposing the semiconductor device to a treatment process, the treatment process selectively removing the compound; and

wherein exposing the semiconductor device to a treatment process comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius while the semiconductor device is exposed to the substantially inert atmosphere to remove the compound.

2. The method of Claim 1, wherein the conductive layer comprises a copper material.

3. The method of Claim 1, further comprising removing the mask layer from the semiconductor device.

4. The method of Claim 3, wherein removing the mask layer comprises removing the mask layer after removing the compound.

5. The method of Claim 3, wherein removing the mask layer comprises removing the mask layer before removing the compound.

6. **(Canceled)** The method of Claim 1, wherein exposing the semiconductor device to a treatment process comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius to remove the compound.

7. The method of Claim 1, further comprising providing a barrier layer between the conductive material and a substrate of the semiconductor device.

8. The method of Claim 1, wherein the conductive material comprises a copper material, and wherein exposing the semiconductor device to a plasma comprises exposing the semiconductor device to a chlorine-containing gas.

9. The method of Claim 8, wherein the compound comprises a copper chloride material, and wherein exposing the semiconductor device to a treatment process comprises exposing the semiconductor device to a hydrogen chloride solution to remove the copper chloride material.

10. The method of Claim 1, wherein the mask layer comprises a photoresist material.

11. **(Amended)** A method for forming a conductive pattern for an electronic device, comprising:

forming a conductive layer outwardly from a substrate of the electronic device;

patterning a mask layer outwardly from the conductive layer, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the electronic device to a plasma **using a plasma deposition reactor and at least one other gas selected from the group of inert gases and nitrogen**, the plasma converting the unmasked portions of the conductive layer into a compound **and the at least one other gas enhancing the conversion into the compound**;

in a separate process from forming the compound, exposing the electronic device to a treatment process to selectively remove the compound;

removing the mask layer from the masked portions of the conductive layer; and

wherein exposing the electronic device to a treatment process comprises:

exposing the electronic device to a substantially inert atmosphere; and

heating the electronic device to between 300 and 800 degrees Celsius while the electronic device is exposed to the substantially inert atmosphere to remove the compound.

12. The method of Claim 11, wherein removing the mask layer comprises removing the mask layer before removing the compound.

13. The method of Claim 11, wherein forming a conductive layer comprises forming a copper layer outwardly from the substrate.

14. The method of Claim 11, wherein the plasma comprises a gas having an element selected from the halogen group of elements.

15. The method of Claim 11, further comprising providing a barrier layer between the conductive layer and the substrate of the electronic device.

16. The method of Claim 11, wherein exposing the electronic device to a plasma comprises controlling the exposure of the electronic device to the plasma to form a substantially perpendicular interface between the masked conductive material and the compound.

17. The method of Claim 11, wherein patterning a mask layer comprises patterning a photoresist layer outwardly from the conductive layer.

18. A method for forming a conductive pattern for an electronic device, comprising:

masking a portion of a conductive layer of the electronic device, the masked portion of the conductive layer defining the conductive pattern;

exposing the electronic device to a plasma and at least one other gas selected from the group of inert gases and nitrogen, the plasma converting an unmasked portion of the conductive layer into a compound and the at least one other gas enhancing the conversion into the compound; and

in a separate process from forming the compound, exposing the electronic device to a treatment process, the treatment process selectively removing the compound.

19. The method of Claim 18, wherein masking a portion of a conductive layer comprises depositing a photoresist layer outwardly from a portion of the conductive layer.

20. The method of Claim 19, further comprising removing the photoresist layer after removing the compound.

21. The method of Claim 19, further comprising removing the photoresist layer before removing the compound.

22. The method of Claim 18, wherein exposing the electronic device to a plasma comprises exposing the electronic device to a plasma, the plasma comprising a gas having an element selected from the halogen group of elements.

23. The method of Claim 22, wherein the plasma comprises a chlorine-containing gas.

24. The method of Claim 22, wherein the plasma comprises a bromine-containing gas.

25. The method of Claim 22, wherein the plasma comprises a fluorine-containing gas.

26. The method of Claim 22, wherein the plasma comprises an iodine-containing gas.

27. The method of Claim 18, wherein exposing the electronic device to a plasma comprises controlling the exposure of the electronic device to the plasma to form a substantially perpendicular interface between the masked conductive material and the compound.

28. The method of Claim 18, wherein the conductive layer comprises a copper material.

29. The method of Claim 28, wherein exposing the electronic device comprises exposing the electronic device to a plasma, the plasma comprising a chlorine-containing gas, the plasma converting the unmasked portion of the conductive layer to copper chloride.

30. The method of Claim 29, wherein exposing the electronic device to a treatment process comprises exposing the electronic device to a hydrogen chloride solution to remove the copper chloride.

31. A method for forming a conductive pattern for a device, comprising:

patterning a mask layer outwardly from a conductive layer of the device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing, by a plasma deposition reactor, the device to a plasma, the plasma converting the unmasked portions of the conductive layer into a compound; and

exposing the device to a treatment process, the treatment process selectively removing the compound.

32. **(Amended)** A method for forming a conductive pattern for a device, comprising:

patterning a mask layer outwardly from a conductive layer of the device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the device to a **[low energy]** plasma **having an energy level of approximately 30 volts or below**, the plasma converting the unmasked portions of the conductive layer into a compound; and

exposing the device to a treatment process, the treatment process selectively removing the compound.